

IN THE CLAIMS

1. - 4. (canceled)

5. (previously presented) A stacked semiconductor chip package comprising:

a substrate having a top surface;

a first chip on the top surface of the substrate and electrically connected to the substrate;

a second chip disposed above the first chip and electrically connected to the substrate and having two opposed longitudinal sides defining a first length; and

a plate between the first chip and the second chip, physically connected to the first chip and the second chip directly by adhesive, and having two opposed longitudinal sides corresponding to the two longitudinal sides of the second chip, the plate defining a second length, the second length being larger than the first length to expose the opposed longitudinal sides of the plate and to expose the adhesive between the plate and the second chip,

wherein the portion of the plate under the second chip is wrapped in the adhesive , and the adhesive is exposed at the corner formed by the plate and second chip along the longitudinal side of the plate.

6. (previously presented) A stacked semiconductor chip package comprising:

a substrate having a top surface;

a first chip on the top surface of the substrate and electrically connected to the substrate;

a second chip disposed above the first chip and electrically connected to the substrate and having two opposed longitudinal sides defining a first length; and

a plate between the first chip and the second chip, connected to the first chip and the second chip, and having two opposed longitudinal sides corresponding to the two longitudinal sides of the second chip, the plate defining a second length, the second length being larger than the first length to expose the opposed longitudinal sides of the plate and to expose a adhesive layer formed between the plate and the second chip, wherein the portion of the plate under the second chip is wrapped in the adhesive layer, and the adhesive layer is exposed at the corner formed by the plate and second chip along the longitudinal side of the plate,

wherein corresponding to the two longitudinal sides of the second chip, the first chip has two opposed longitudinal sides defining a third length, and the third length is larger than the second length.

7. (previously presented) A stacked semiconductor chip package comprising:

a substrate having a top surface;

a first chip on the top surface of the substrate and electrically connected to the substrate;

a second chip disposed above the first chip and electrically connected to the substrate and having two opposed longitudinal sides defining a first length; and

a plate between the first chip and the second chip, connected to the first chip and the second chip, and having two opposed longitudinal sides corresponding to the two longitudinal sides of the second chip, the plate defining a second length, the second length being larger than the first length to expose the opposed longitudinal sides of the plate and to expose a

adhesive layer formed between the plate and the second chip, wherein the portion of the plate under the second chip is wrapped in the adhesive layer, and the adhesive layer is exposed at the corner formed by the plate and second chip along the longitudinal side of the plate,

wherein corresponding to the two longitudinal sides of the second chip, the second chip further has two opposed transverse sides defining a first width, the plate further has two opposed transverse sides defining a second width, the second width is smaller than the first width.

8. (previously presented) The stacked semiconductor chip package according to claim 7, wherein the first chip further has two opposed transverse sides defining a third width, and the second width is smaller than the third width.

9. (previously presented) The stacked semiconductor chip package according to claim 6, wherein corresponding to the two longitudinal sides of the second chip, the second chip further has two opposed transverse sides defining a first width, the plate further has two opposed transverse sides defining a second width, the second width is smaller than the first width.

10. (previously presented) The stacked semiconductor chip package according to claim 9, wherein the first chip further has two opposed transverse sides defining a third width, and the second width is smaller than the third width.

11. (canceled)